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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,667	11/20/2001	Francis Joseph	10003432-1	1779

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EXAMINER
MASON, DONNA K

ART UNIT	PAPER NUMBER
2111	2

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,667	JOSEPH, FRANCIS	
	Examiner	Art Unit	
	Donna K. Mason	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 7, line 25, insert --in-- after "stored".

Appropriate correction is required. See 37 CFR 1.71.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 7 recites the limitation "the ferroelectric memory component *embedded* in the re-configurable hardware" (emphasis added) in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2002/0129191 to DaCosta.

With regard to claims 1 and 8, DaCosta discloses a system including: a system bus (Fig. 1, item 100); a processor (Fig. 1, item 101) in communication with the system bus; an input/output (I/O) interface (Fig. 1, item 108) in communication with the system bus; and a ferroelectric memory component (Fig. 1, items 102 and 103; paragraphs [0027] and [0031]) in communication with the system bus. DaCosta also discloses the system where the ferroelectric memory component is a ferroelectric random access memory (FeRAM) component (paragraph [0031]).

DaCosta does not expressly use of a system-on-chip (SOC) architecture, as recited in independent claim 1. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to use a SOC architecture, thereby placing the entire system on a single IC. Applicant has not disclosed that the use of a SOC architecture provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art would have expected Applicant's invention to perform equally well without the SOC architecture because the system elements' ability to perform their individual functions would not be affected by their location on a single IC.

Furthermore, as held in *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965), making a system integral would merely be a matter of design choice. In that case, a claim to a fluid transporting vehicle was rejected as obvious over a prior art reference, which differed from the prior art in claiming a brake drum integral with a

clamping means, while the brake disc and clamp of the prior art included several parts rigidly secured together as a single unit. The court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice."

Therefore, it would have been obvious to one of ordinary skill in this art to modify DaCosta to obtain the invention as specified in claims 1 and 8.

7. Claims 1-4, 8-10, and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("APA") in view of DaCosta.

With regard to claim 1, the APA discloses a System-On-Chip (SOC) architecture (Fig. 1, item 1) including: a system bus (Fig. 1, item 10); a processor (Fig. 1, item 2) in communication with the system bus; and an input/output (I/O) interface (Fig. 1, item 7) in communication with the system bus.

With regard to claims 2-4, the APA discloses the SOC, further including debugging and self-test modules (Fig. 1, item 9) in communication with the system bus, a direct memory access (DMA) component in communication with the system bus, and a memory controller in communication with the system bus.

With regard to claims 9 and 10, the APA discloses the SOC, where the processor is a microprocessor, and where the processor is a microcontroller (Fig. 1, item 2, and page 1, line 24).

With regard to claims 15-19, the APA discloses the SOC, further including an intellectual property (IP) hardware component (Fig. 1, item 3) in communication with the system bus, an input/output (I/O) hardware component (Fig. 1, item 6) in communication

with the system bus, a static random access memory component (Fig. 1, item 4), and a dynamic random access memory (DRAM) component (Fig. 1, item 4).

The APA does not expressly disclose a ferroelectric memory component in communication with the system bus, as recited in independent claim 1, or the SOC where the ferroelectric memory component is a ferroelectric random access memory (FeRAM) component, as recited in claim 8.

DaCosta discloses a ferroelectric memory component (Fig. 1, items 102 and 103; paragraphs [0027] and [0031]) in communication with a system bus, and a system where the ferroelectric memory component is a ferroelectric random access memory (FeRAM) component (paragraph [0031]).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine DaCosta with the APA. The suggestion or motivation for doing so would have been to reduce the time to bootup and shutdown a computer system. The time to bootup the computer system and open an application is reduced because respectively, the operating system and the application software do not need to be copied into RAM and initialized into an executable state. The time to shutdown the computer system is reduced because it is not necessary to back up information from RAM to non-volatile memory (paragraph [0015]).

Therefore, it would have been obvious to combine DaCosta with the APA to obtain the invention as specified in claims 1-4, 8-10, and 15-18.

8. Claims 5-7, 11-14, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over DaCosta in view of U.S. Patent No. 6,145,020 to Barnett.

As described above with regard to the 35 U.S.C. 103(a) rejection of independent claim 1, the features of claim 1 are obvious in view of DaCosta.

With regard to claims 5-7, DaCosta does not expressly disclose re-configurable hardware in communication with the system bus, where the re-configurable hardware has a ferroelectric memory component embedded therein, where the re-configurable hardware has a configuration that is stored in the ferroelectric memory component embedded in the re-configurable hardware, and where the ferroelectric memory component embedded in the re-configurable hardware is a ferroelectric random access memory (FeRAM) component.

Barnett discloses re-configurable hardware (Fig. 4, item 84'), where the re-configurable hardware has a ferroelectric memory component (Fig. 4, item 154) embedded therein, where the re-configurable hardware has a configuration (Fig. 4, item 152) that is stored in the ferroelectric memory component embedded in the re-configurable hardware, and where the ferroelectric memory component embedded in the re-configurable hardware is a ferroelectric random access memory (FeRAM) component (Fig. 4, item 154).

With regard to claims 11-14, DaCosta does not expressly disclose all the features of those claims. Barnett discloses a ferroelectric memory component (Fig. 3, item 138; and column 6, lines 53-67 to column 7, lines 1-13) that stores programs and data needed by the processor for execution of the programs by the processor, and where, during execution of a program by the processor, the processor causes an instruction pointer to be stored in a predetermined location in the ferroelectric memory

component that identifies a location in the ferroelectric memory component that contains an address of a next instruction to be executed by the processor (column 7, lines 1-67 to column 8, lines 1-8).

With regard to claims 12-14 and 19-22, Barnett discloses a re-configurable hardware component, where the processor causes the configuration of the re-configurable hardware component to be stored in the ferroelectric memory component (column 8, lines 2-8), and when the re-configurable hardware is executing, current state values of the re-configurable hardware are stored at predetermined locations in the ferroelectric memory component, and wherein if a power cycle occurs, then when power returns, the processor uses the instruction pointer to obtain the next instruction to be executed and resumes execution of the program, and where if a power cycle occurs, when power returns, said current state values are read out of the ferroelectric memory component and used by the re-configurable hardware to resume execution of the re-configurable hardware (column 7, lines 50-59).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Barnett with DaCosta. The suggestion or motivation for doing so would have been to increase the ability to quickly load different configuration data sets for different peripherals (column 2, lines 25-29; and column 8, lines 39-67 to column 9, lines 1-4).

Therefore, it would have been obvious to combine Barnett with DaCosta to obtain the invention as specified in claims 5-7, 11-14, and 19-22.

Conclusion

9. A shortened statutory period for reply is set to expire THREE MONTHS from the mailing date of this communication. Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this communication.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (703) 305-1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKM

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